IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

SYNOPSYS, INC., a Delaware Corporation, Plaintiff and Counter-Defendant, v. MAGMA DESIGN AUTOMATION, a Delaware Corporation, Defendant and Counterclaimant. AND RELATED COUNTERCLAIMS.	C.A. No. 05-701 GMS

DECLARATION OF EDMOND S. COOLEY, D. Eng.

I, Edmond S. Cooley, have personal knowledge of all the facts and opinions contained herein and, if called to testify, could and would competently testify thereto.

1. I am currently an Associate Professor of Engineering, Senior Lecturer, and Chief Information Technology Strategist at Dartmouth College.

2. I have earned a bachelor degree in electrical engineering from the University of Vermont in 1980, and master and doctoral degrees from the Thayer School of Engineering at Dartmouth College, in 1982 and 1988, respectively.

3. I have worked in VLSI circuit design for Raytheon Company and Aerodyne Research, and have consulted with a number of companies in hardware and software development, design, test, and implementation.

4. I have authored or co-authored more than 30 articles and abstracts on system design including electronic design automation, hardware description languages, artificial intelligence, circuit test, communications, and networking.

5. I have taught both graduate and undergraduate courses in circuit design, systems design including electronic design automation, hardware description languages, and communications theory. I have done research in Design for Test (DFT), VLSI Design, and wired and wireless networking.

6. I am a member of Institute of Electrical and Electronics Engineers (IEEE), American Society for Engineering Education (ASEE), the American Association for Artificial Intelligence, the Association for Computing Machinery, and the Society of Photo-Optical Instrumentation Engineers. My resume is attached as Exhibit A.

7. I have reviewed U.S. Patent No. 6,192,508 ("'508 Patent").

8. In my opinion, the '508 Patent does not describe a bin and there is no definition of a "bin" anywhere in the '508 Patent. While Figs. 5a and 5b show a diagram including bins, the bins are indicated by dashed lines and therefore do not give information about the location or orientation of the given circuitry on the chip. Further, the diagrams are logical diagrams rather than schematic or physical layouts, which would show the actual locations of the logic cells on the chip.

9. In my opinion, one of ordinary skill in the art of EDA, in June of 1998, would have understood a "bin" to be a "rectangular (or square) portion of an integrated circuit bounded by gridlines."

10. In 1998, bins were commonly described in connection with the Min-Cut placement technique which divides the cells of a chip and places them into smaller and smaller bins using cut-lines or gridlines. Thus, the bins were either squares or rectangles. Also, at that point in time, it was recognized that some bins could be larger than others, for example, by making one large square bin out of four smaller square bins. The "larger" bin would still be bounded by the gridlines of the smaller bins.

11. The Min-Cut algorithm is more of a brute-force algorithm that does not analyze the system as a whole, but rather identifies individually congested bins and uses placement to reduce the congestion in the more congested bins (either by adjusting the placement within the bin, or moving components in a congested bin to a less congested bin).

12. In 1998, the term bins was not commonly used at the time to describe floor-planning regions, which could be square, rectangular, or irregularly shaped regions or polygons, that are not constrained to follow gridlines. Therefore, it is my opinion that in June of 1998 one of ordinary skill in the art would have understood a bin to be a rectangular (or square) portion of an integrated circuit bounded by gridlines.

13. To my knowledge in 1998, Min-Cut placement was the most widely-adopted placement procedure for automated chip design.

14. By 1998, Min-Cut had been used by industry for over 10 years.

15. In June of 1998, a new and competing cell placement approach called the "Force-Directed" technique was published in the proceedings of DAC, the world's largest EDA conference. [Exhibit B, "Generic Global Placement and Floorplanning," Proceedings of the 35th Design Automation Conference, pps. 269-274, 1998.] The Force-Directed approach did not use bins, and became popular in EDA systems.

16. The '508 patent does not mention or acknowledge the Force-Directed approach. Rather, it teaches an incremental improvement to partition-based placement algorithms (such as the Min-Cut algorithm), which were widely adopted at the time that the '508 patent was filed.

17. The '508 patent repeatedly discusses the use of partitioning and bins -- neither of which are used in the forced directed approach -- and discusses how logic optimization can be used to improve congestion within a bin or between bins.

18. The '508 Patent discloses a method for calculating congestion: the number of pins in a bin divided by the routable area of the bin. ('508 Patent, col. 4, ll. 53-55.) If

a single bin covered an entire chip, that method for calculating congestion would give useless information about congestion, providing no indication of the location of congested areas on the chip.

19. In the '508 Patent, the term "selected bins" means "more than one bin selected based on congestion" because "bins" is plural and because the specification teaches that "selected" bins are selected "based on congestion."

20. Prior to 1998, logic modifications had been performed to improve timing in parts of the circuit. In my opinion, these timing improvements necessarily reduce a constraint on the layout of the chip and allow cells to be moved around on the chip. This is because the timing improvements create some timing slack, which provides placement flexibility. Because "logic modifications to improve timing" inherently reduce constraints on any subsequent placement step, I understand the requirement of "reducing constraints on a subsequent placement step" in the claims of the '508 Patent to mean, in light of the specification, reducing constraints with the purpose of reducing congestion during the subsequent placement steps.

21. The '508 patent recognizes that there are certain timing criteria that must be met and which might be affected by logic modifications. Further, it teaches that, after identifying congested circuits and cells that must be modified in order for placement to relieve congestion, but before the logic modifications are made to improve congestion, the logic is modified in order to improve timing slack in that part of the circuit, *e.g.* at Col. 3 at ll. 59-67 and Col. 4 at ll. 3-7.

22. Every time the word "constraint" is used in the '508 Patent, it is used as the plural "constraints."

23. Every time the word "limit" is used in the '508 Patent, it is used as the plural "limits."

24. The word "congestion" appears 56 times in the nine pages of the '508 Patent.

I declare under penalty of perjury that the foregoing is true and correct.

DATED: November 3, 2006

EDMOND S. COOLEY

CERTIFICATE OF SERVICE

I hereby certify that on November 3, 2006, I electronically filed with the Clerk of Court the foregoing **Declaration of Edmond S. Cooley, D.Eng.** using CM/ECF which will send electronic notification of such filing(s) to the below-listed Delaware counsel. In addition, the filing will also be sent via hand delivery to:

Karen Jacobs Louden, Esquire Morris, Nichols, Arsht & Tunnell 1201 North Market Street Wilmington, DE 19801	Attorneys for Plaintiff Synopsys, Inc.

I hereby certify that on November 3, 2006, I have mailed by United States Postal Service, the document(s) to the following non-registered participants:

Valerie M. Wagner, Esquire Dechert LLP 1117 California Avenue Palo Alto, CA 94304	Attorneys for Plaintiff Synopsys, Inc.

/s/ Kyle Wagner Compton
Kyle Wagner Compton